

CLAIMS

What is claimed is:

- 5 1. A method of protecting a microelectronic device during one or more release etch steps, the method comprising:
- a) providing a microelectronic device having a passive area and an active area;
- b) applying an electrically insulating protective coating to at least some of the passive area, but not to the active area; and
- 10 c) performing at least one release etch step to release the active area.
2. The method of claim 1, wherein the protective coating comprises a thin, vapor-deposited parylene polymer.
- 15 3. The method of claim 2, wherein the parylene coating comprises at least one material selected from the group consisting of poly-para-xylylene, poly-para-xylylene that has been modified by the substitution of a chlorine atom for one of the aromatic hydrogens, and poly-para-xylylene that has been modified by the substitution of the chlorine atom for two of the aromatic hydrogens.
- 20 4. The method of claim 1, wherein the protective coating comprises an epoxy based negative photoresist that is resistant to acids and solvents, and which has a low viscosity in the liquid form.
- 25 5. The method of claim 4, wherein the photoresist comprises SU-8 or SU-8 2000.
6. A microelectronic device, comprising:
- an electrically insulating substrate;
- a first electrical conductor disposed on the substrate;
- 30 a microelectronic device attached to the substrate, wherein the device comprises an active area and a passive area;
- a second electrical conductor disposed on the device, located within the passive area;

an electrical interconnection made between the first and second electrical conductors;
and
an electrically insulating, protective coating covering the first and second electrical
conductors, the electrical interconnection, and the passive area; but not covering the
active area.

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7. The microelectronic device of claim 6, wherein the substrate comprises one or more
electrically insulating materials selected from the group consisting of ceramic, plastic, printed
wiring board material, polymer, multi-layered material, LTCC ceramic multilayered material,
and HTCC ceramic multilayered material.

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8. The microelectronic device of claim 6, wherein the substrate comprises a package having a
geometry selected from the group consisting of DIP, Ceramic DIP, CERDIP, quad flatpack, pin
grid array, leadless chip carrier, and a leaded flatpack.

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9. The microelectronic device of claim 6, further comprising one or more active elements,
disposed within the active area, selected from the group consisting of MEMS elements,
optically sensitive elements, temperature sensitive elements, heat sensitive elements,
chemical sensitive elements, pressure sensitive elements, and microsensors.

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10. The microelectronic device of claim 6, further comprising one or more released MEMS
elements disposed within the active area.

11. The microelectronic device of claim 6, further comprising one or more unreleased MEMS
elements disposed within the active area.

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12. The microelectronic device of claim 6, wherein the electrical interconnection comprises a
wirebond or a flip-chip ball or bump.

13. The microelectronic device of claim 6, wherein the device is flip-chip mounted to the
substrate, and wherein the substrate comprises an aperture aligned over the active area,
whereby the active area is accessible through the aperture.

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14. The microelectronic device of claim 6, wherein the package comprises a transparent window disposed across the aperture.

5 15. The microelectronic device of claim 6, wherein the electrically insulating protective coating comprises one or more materials selected from the group consisting of a vapor-deposited coating, a vacuum vapor deposited coating, a chemical vapor deposited coating, a water-insoluble coating, a water-soluble coating, a dry-etchable coating, a conformal coating, a pin-hole free coating, parylene, a photopatternable/photoimaggable material, photoresist, a low
10 viscosity photoresist, an epoxy based negative resist, SU-8, SU-8 2000, a sputtered coating, an evaporated coating, a ceramic coating, silicon nitride, aluminum oxide, mullite, a sprayed coating, a self-assembled monolayered material, cyanoacrylate, perfluoropolyether, hexamethyldisilazane, perfluorodecanoic carboxylic acid, silicon dioxide, TEOS, silicate glass, a fast-etch glass, silicon, and polysilicon.

15 16. The microelectronic device of claim 6, wherein the electrically insulating protective coating comprises one or more materials selected from the group consisting of poly-para-xylylene, poly-para-xylylene that has been modified by the substitution of a chlorine atom for one of the aromatic hydrogens, and poly-para-xylylene that has been modified by the substitution of the
20 chlorine atom for two of the aromatic hydrogens.

17. The microelectronic device of claim 6, wherein the passive area comprises an integrated circuit.

25 18. The microelectronic device of claim 6, further comprising an electrically conductive overcoat deposited on top of the electrically insulating protective coating, whereby the electrically conductive overcoat provides electromagnetic shielding.

30 19. The microelectronic device of claim 18, wherein the electrically conductive overcoat comprises one or more conductive materials selected from the group consisting of a metal, gold, tungsten, nickel, aluminum, copper, titanium, molybdenum, tin, tantalum, a metal alloy, an electrically-conductive polymer, carbon, doped carbon, and doped silicon.

20. The microelectronic device of claim 6, wherein the conductive overcoat is continuous across two or more adjacent electrical interconnections.

5 21. The microelectronic device of claim 6, wherein the electrical interconnection is not encapsulated by a bulk encapsulant.

22. The microelectronic device of claim 6, wherein the substrate comprises an interposer or an interposer with an aperture aligned with the active area.

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23. A method of fabricating a microelectronic assembly, comprising:

a) providing an assembly comprising:

a microelectronic device attached to an electrically insulating substrate, and
a first electrical conductor disposed on the substrate;

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wherein the microelectronic device comprises an active area, a passive area, and a
second electrical conductor disposed on the device within the passive area; and
an electrical interconnection made between the first and second electrical
conductors; and then

b) applying an electrically insulating, protective coating on to at least the first and second
20 electrical conductors, the electrical interconnection, and at least some of the
passive area; while preventing the protective coating from being deposited on to
the active area.

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24. The method of claim 23, wherein the microelectronic device comprises one or more
unreleased MEMS elements disposed within the active area; and wherein the method further
comprises: c) releasing the unreleased MEMS elements after applying the protective coating
in step b), without removing the protective coating from the passive area.

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25. The method of claim 24, wherein the protective coating is resistant to HF or HCL acid, and
wherein the step of releasing the MEMS elements comprises using a wet etching solution
comprising HF, HCL, or a mixture of both.

26. The method of claim 23, wherein preventing the protective coating from being deposited on to the active area in step b) comprises:

i) compressing an elastomeric plug on to the active area before applying the protective coating in step b); and then

5 ii) removing the elastomeric plug after the protective coating has been applied in step b).

27. The method of claim 23, wherein preventing the protective coating from being deposited on to the active area in step b) comprises:

i) attaching a patch of temporary material to the active area before applying the protective
10 coating in step b); then

ii) performing step b); then

iii) removing any portion of the protective coating that was applied on to the patch of temporary material; and

15 iv) removing the patch of temporary material from the active area, thereby exposing the active area.

28. The method of claim 27, wherein step iii) comprises using one or more material removal techniques selected from the group consisting of laser ablation, plasma etching, cutting the perimeter with a knife or a laser, mechanical abrasion, scuffing, slicing, and scratching.

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29. The method of claim 27, wherein steps iii) and iv) are performed simultaneously.

30. The method of claim 27, wherein the patch of temporary material comprises one or more materials selected from the group consisting of an adhesive tape, a non-adhesive tape,

25 Teflon® tape, a polymer glob, a latex glob, a water-soluble coating, starch, sugar, and an acid-etchable material.

31. The method of claim 23, wherein applying the protective coating in step b) comprises covering the active area with a mask; and then using a line-of-sight coating technique to apply
30 the protective coating to the passive area; whereby the mask prevents the protective coating from being deposited on to the active area.

32. The method of claim 30, wherein the line-of-sight coating technique comprises one or more techniques selected from the group consisting of sputtering, spraying, evaporating, streaming, globbing, dabbing, dispensing, and ablating.

5 33. The method of claim 22, further comprising applying an electrically conductive overcoat on top of the electrically insulating protective coating to provide shielding from electromagnetic interference.

34. The method of claim 22, wherein the microelectronic device is flip-chip mounted to the
10 substrate, and further wherein applying the protective coating in step b) comprises underfilling the flip-chip interconnections with a polymer to form a continuous ring seal.

35. The method of claim 22, wherein providing the assembly in step a) comprises:

- 15 i) providing an unreleased die comprising a silicon substrate; an active area comprising MEMS elements disposed on the silicon substrate; a passive area comprising bond pads and conductive lines disposed on the silicon substrate; and further comprising a sacrificial layer covering both the active and passive areas, wherein the MEMS elements are unreleased; then
- 20 ii) applying a glob of protective material on to the active area, but not the passive area; then
- iii) removing that portion of the sacrificial layer that covers the passive area; and then
- iv) removing the glob of protective material from the active area, thereby exposing the sacrificial layer covering the active area, before starting step b).

25 36. A method of fabricating a microelectronic assembly, comprising:

- a) providing an assembly comprising:
 - a microelectronic device attached to an electrically insulating substrate, and
 - a first electrical conductor disposed on the substrate; wherein the microelectronic device comprises an active area, a passive area, and a second electrical
 - 30 conductor disposed on the device within the passive area; and
 - an electrical interconnection made between the first and second electrical conductors; and then

- b) applying an electrically insulating, protective coating on to at least the first and second electrical conductors, the electrical interconnection, at least some of the passive area, and the active area of the device; and then
- c) removing the protective coating from the active area of the device, without removing
5 the protective coating from the passive area.

37. The method of claim 36, wherein the microelectronic device comprises one or more unreleased MEMS elements disposed within the active area; and wherein the method further comprises releasing the unreleased MEMS elements after removing the protective coating
10 from the active area of the device in step c).

38. The method of claim 36, further comprising:

- i) after step b), placing a mask over the passive area of the device and any other surfaces of the assembly where the protective coating should remain, wherein the
15 mask does not cover the active area; and then
- ii) removing the electrically insulating protective coating using a line-of-sight removal technique from areas of the assembly not covered by the mask, including the active area, while not removing the protective coating from the areas that are occluded by the mask, thereby exposing the active area.

39. The method of claim 38, wherein the line-of-sight removal technique comprises plasma etching.

40. The method of claim 38, wherein the microelectronic device provided in step a) comprises
25 one or more unreleased MEMS elements disposed within the active area; and further wherein the one or more unreleased MEMS elements are temporarily encased in a sacrificial vapor-deposited encapsulant; and additionally wherein the method comprises re-releasing the one or more unreleased MEMS elements by removing the sacrificial vapor-deposited encapsulant after removing the electrically insulating protective coating and exposing the active area in
30 step ii).

41. The method of claim 40, wherein the sacrificial vapor-deposited encapsulant comprises a parylene polymer.

5 42. The method of claim 36, wherein removing the protective coating in step c) comprises ablating the protective coating from the active area of the device with a laser.

43. The method of claim 38, wherein the microelectronic device is flip-chip mounted to the substrate; and wherein the substrate comprises an aperture aligned with the active area, whereby the active area is accessible through the aperture; and further wherein the aperture
10 provides access for removing the protective coating from the active area by using a line-of-sight removal technique during step ii); whereby the substrate serves as a natural mask for occluding those surfaces of the assembly where the protective coating should remain during the line-of-sight removal in step ii).

15 44. The method of claim 36, wherein the protective coating comprises a negative-type photoresist material, and wherein removing the protective coating from the active area of the device while not removing the protective coating from the passive area in step c) comprises:
i) masking the active area, but not the passive area; then
ii) exposing the masked assembly; and then
20 iii) developing the photoresist material; whereby the unexposed portion of the photoresist material is removed from the active area.

45. The method of claim 44, wherein the photoresist material comprises SU-8 or SU-8 2000.

25 46. The method of claim 36, wherein the substrate comprises at least one of the following selected from the group consisting of a package, an interposer, and an interposer with an aperture aligned with the active area.

47. The method of claim 36, wherein providing the assembly in step a) comprises:
30 i) providing an unreleased die comprising a silicon substrate; an active area comprising MEMS elements disposed on the silicon substrate; a passive area comprising bond pads and conductive lines disposed on the silicon substrate; and

further comprising a sacrificial layer covering both the active and passive areas,
wherein the MEMS elements are unreleased; then

ii) applying a glob of protective material on to the active area, but not the passive area;
then

5 iii) removing that portion of the sacrificial layer that covers the passive area; and then
iv) removing the glob of protective material from the active area, thereby exposing the
sacrificial layer covering the active area, before starting step b).